

# NGUYEN VIET KHANG

ELECTRICAL-ENGINEERING

CONTROL ENGINEERING AND AUTOMATION



## CONTACT

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## EDUCATION

2022-PRESENT

HCM International University

- Automation-Electrical Engineering
- GPA: 3.53/4.0 last semester and 3.35/4.0 overall
- IELTS certification 6.5

## SKILLS

- Hard-working
- Time management
- Multitasking
- System modelling and optimization
- C/C++, Python, Verilog, VHDL, SystemVerilog
- Altium, Matlab, Solidworks
- Known the End-to-End ASIC Flow

## LANGUAGES

- English (Fluent)

## PROFILE

An motivated Automation and Electrical Engineering student with hands-on experience in IoT systems, PLC, and embedded C development. familiar with integrating hardware and software solutions for industrial and smart system projects, eager to apply experiences and technical skills in real-world engineering environment.

## PROJECTS

○ **Double hull automatic trash collecting boat** 11/11/2024-23/06/2025

### Capstone 2 's project

- Fabricate and design general structure of boat with Solidworks
- Program Auto-tuned PID control algorithm and kalman filter for the stability of boat
- optimizing code for better control protocols and responses
- monitor boat 's responses for better PID tuning and controlling

### **Digital Signal Processing (DSP) Hardware:**

○ **Parameterizable FIR/IIR Filter** 28/04/2025-03/06/2025

### Digital Signal Processing Project

- Write Verilog/SystemVerilog to implement a Finite Impulse Response (FIR) or Infinite Impulse Response (IIR) filter
- Verification: Write a testbench to feed a noisy digital signal into RTL filter, capture the output, and prove that it successfully filtered the signal according to mathematical model.

### **Hardware Control Systems: Stepper Motor & Sensor**

○ **Controller use FPGA**

### Microprocessing Projects

12/11/2025--26/05/2026

- Design an RTL module that generates precise, high-speed PUL/DIR timing signals for a stepper motor driver.
- Integrate this with a hardware SPI controller to read live data from an ADC reading a load cell

### **A Pipelined Processor Core (RISC-V)**

### Embedded system Projects

2/10/2026--26/05/2026

- Design a basic 3-stage or 5-stage pipelined microprocessor using the open-source RISC-V instruction set.
- design the Arithmetic Logic Unit (ALU), the register file, instruction memory



## WORKS EXPERIENCES

Have worked at private electronics company, I have developed strong practical skills through academic university projects and company internship involving embedded systems, optimize and modelling an system, design layout and fabricate PCB.